ABSTRACT

Systems for reducing the parasitic effects of a transistor-based switch are provided. In one such system provides a transistor circuit for implementing a switch having reduced parasitic effects. In general, the transistor circuit comprises a first switch node, a second switch node, a third switch node, a transistor device, and a circuit configured to reduce the parasitic characteristics of the transistor device. The first switch node is for connecting to one node of an external circuit. The second switch node is for connecting to a second node of an external circuit. The transistor device is a three-terminal device. The first terminal is connected to the first switch node. The second terminal is connected to the second switch node. The third terminal is for receiving a control signal that operates the transistor circuit as a switch by controlling the electrical connectivity between the first terminal and the second terminal. The third switch node is for receiving the control signal. The transistor circuit may also comprise an inverter circuit that is connected to the second terminal of the transistor device and is configured to provide a voltage to the second terminal when the control signal engages the transistor device.